

4-Port Parallel I/O Board (88-4PIO)

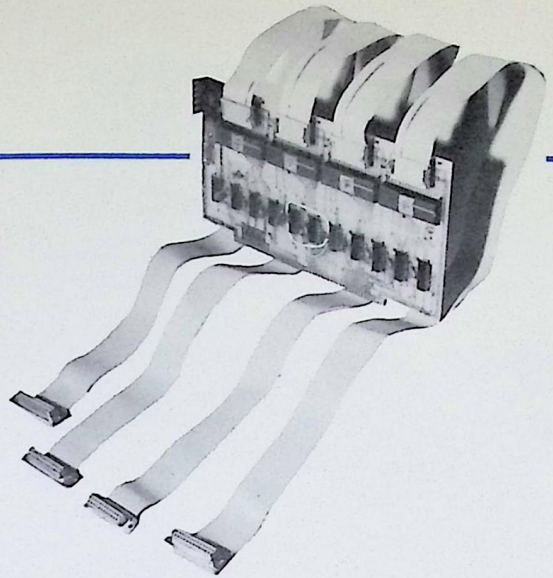
The 88-4PIO board design is based upon a peripheral interface integrated circuit. The chip contains all control and data registers, thus most 88-4PIO options are software selectable. These options include data direction (each data line can act as input or output) and interrupt/control structure modification. The 88-4PIO board can be expanded to four "PORTS" (four 6820 ICs), making it one of the most powerful and versatile interface boards available.

Hardware

The 4PIO board connects to the back panel of the computer with a removable flat cable. The cable has a 24-pin removable plug on the board, and a 25-pin connector on the back panel.

Altair slots: One.

Power: + 5 volts at 500 milliamps with 4 ports.



Capabilities

The 4PIO board is capable of handling up to 4 ports on one plug-in card. Each port contains 16 data lines. Each line can be initialized as input or output to interface a terminal (8 lines in, 8 lines out).

The 4PIO board can handle 2 inputs (such as a paper tape reader and keyboard) or two output devices (such as a paper tape punch and printer) or any combination of custom applications.

All data lines are fully TTL compatible. Eight of the 16 lines are capable of directly driving the base of a transistor switch (1.5V at 1 ma).

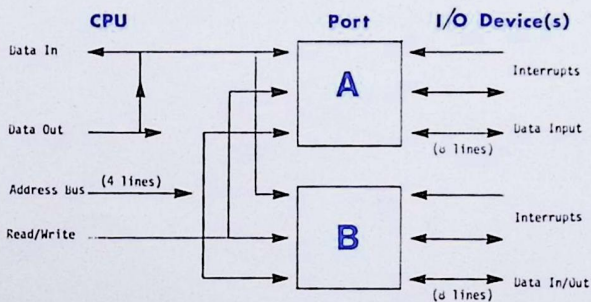
A 4PIO with 4 ports has 64 data lines (each group of 8 is individually selectable) and consumes 500 ma at 5V—typical.

Interface—Parallel; 16 data lines, 4 control/interrupt lines; TTL compatible input and output, plus 8 of the 16 data lines can drive 1.5 volts at 1 milliamp for transistor compatibility.

Bit Configuration : Each data line can be software selected to act as an input or output.

Operation

Each port provides 4 controllable handshake lines. These lines are enabled/disabled under software control. Two interrupt lines are capable of acting as outputs for ready/busy handshake. There are 2 control/status registers which contain a status bit for each of the 2 interrupt lines to the CPU. The following simplified block diagram demonstrates the address-register operation of one port on the 88-4PIO:



Assuming that the board is addressed at location 0, register selection for port 0 is:

Address	Register
0	Section A—Control
1	Section A—Data
2	Section B—Control
3	Section B—Data

Port 1 includes addresses 4, 5, 6, and 7;
Port 2 includes addresses 8, 9, 10, and 11;
Port 3 includes addresses 12, 13, 14, and 15.

Control/Status—Each 8-bit section:
a. Input : sets flag and/or interrupt line
b. Input: acts as above
Output: acts as "busy" signal back to the device.

Interrupt Structure—Each 8-bit section:
a. Interrupt request signal to CPU or 88-VI.
b. 2 interrupt status bits, 1 for each of above control lines.

Address Select—Each port requires 4 addresses.